| Branch: BCA | Semester-III |
|---|---|
| Subject Code: 3104 | Lecture: 04<br>Credit: 04 |
| Course Opted | Core Course - 10 |
| Subject Title | COMPUTER ORGANISATION AND ARCHITECTURE |

**Course Objectives:**

- To introduce fundamental concepts of Boolean algebra, logic gates and combinational circuits
- To give a basicunderstanding of concepts and structure of computers.
- To understand the organization of Cache memory and memory management hardware.
- To study the working of different interrupts & Mapping Techniques.
- To study register organization.
- To understand the different addressing modes.
- To Demonstrate the working of central processing unit and RISC and CISC Architecture.

**Course Outcomes:**

- Understand the architecture and functionality of central processing unit.
- Analyze some of the design issues in terms of speed, technology, cost, performance.
- Learn the concepts of parallel processing, pipelining and inter-processor communication.
- Exemplify the I/O and memory organization.

| Modules | Sr. No. | Topic and Details | No. of Lectures Assigned | Marks Weightage % |
|---|---|---|---|---|
| **UNIT –I** | 1 | **Basic Structure of computers:**<br>Comparison of Computer Organization & Architecture, Structure and function, evolution of Intel x86 Architecture, Basic Measures of Computer Performance, Computer Components, Computer Function (Instruction Cycle, Interrupts), Interconnection Structures, Bus Interconnection, Peripheral Component Interconnection (PCI). | 8 | 16 |
| **UNIT – II** | 2 | **Memory Organization:**<br>**Cache Memory:**<br>Computer Memory System Overview, Cache Memory Principles, Elements of cache design (Size, Mapping, Replacement, Write policies, Block size)<br>**Internal Memory:**<br>Semiconductor Main memory, Error detecting & correcting codes | 7 | 14 |
| | 3 | **Input/Output:** External devices, I/O Modules, Programmed I/O, Interrupted-Driven I/O, Direct Memory Access | 7 | 14 |
| **UNIT – III** | 4 | **Arithmetic and Logic:**<br>Computer Arithmetic, Integer representation, Floating point representation<br>**Digital Logic :**<br>Boolean algebra, Gates | 8 | 16 |

| | | | | |
|---|---|---|---|---|
| | 5 | **Central Processing Unit:**<br>Instruction sets : Instruction characteristics, Types of operands, Types of operations, addressing modes Processor Organization, Register organization, Instruction cycle. | 12 | 24 |
| **UNIT –IV** | 6 | **RISC:**<br>Instruction Execution Characteristics, RISC characteristics and RISC Pipelining, RISC Vs.CISC<br>**Parallel organization:**<br>Multiple processor organizations (SISD, SIMD, MISD and MIMD) | 8 | 16 |
| **Total** | | | **50** | **100** |

**Text Book:**

1. William Stallings “Computer Organization and Architecture” , Prentice Hall, 10th Edition

**References:**


1. Douglas V. Hall, “Microprocessor and Interfacing”, Tata McGraw-Hill 2nd Edition
2. Barry B. Brey, “The Intel Microprocessors 8086/8088…”, PHI, 4th Edition
3. Morris Mano, “Computer System Architecture”, Pearson Custom Publishing, 2001
4. Hwang, “Advanced Computer Architecture”, Tata McGraw Hill Education, 2003
5. Michael J. Flynn, “Computer Architecture”, Narosa Publishing, 1995
6. P.R. Devale, “Computer Organisation and Architecture”, 2004